Figure 1

Figure 2

Figure 3

Instruction Dispatch Signals

300

| CPU | 302 | 312 | 316 | COPx | 310 |

CP_ir_m[31:0]
CPx_as_m
CPx_ts_m
CPx_fs_m
CP_VNs_m
CP_VN_m

CP_order_m[2:0]

CPx_abusy_m
CPx_tbusy_m
CPx_fbusy_m

Figure 4

400

Instruction Transfer

Clock

CP_ir_m[31:0]   A   B   C

CPx_as_m

CPx_ts_m

CPx_fs_m

Instruction Valid or Null

CP_VNs_m

CP_VN_m

Figure 5

/ 500
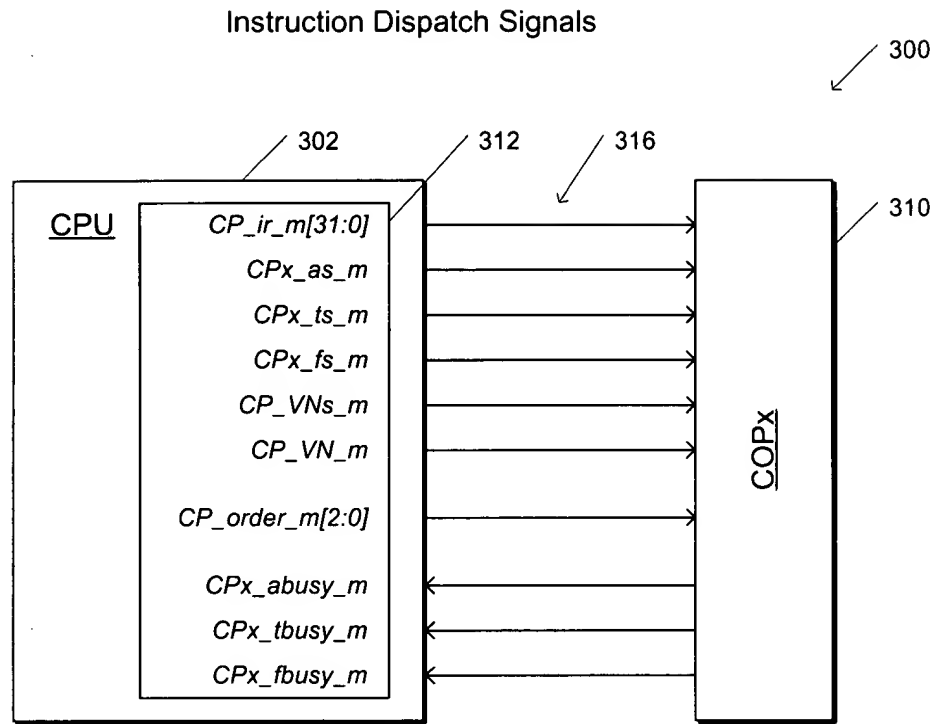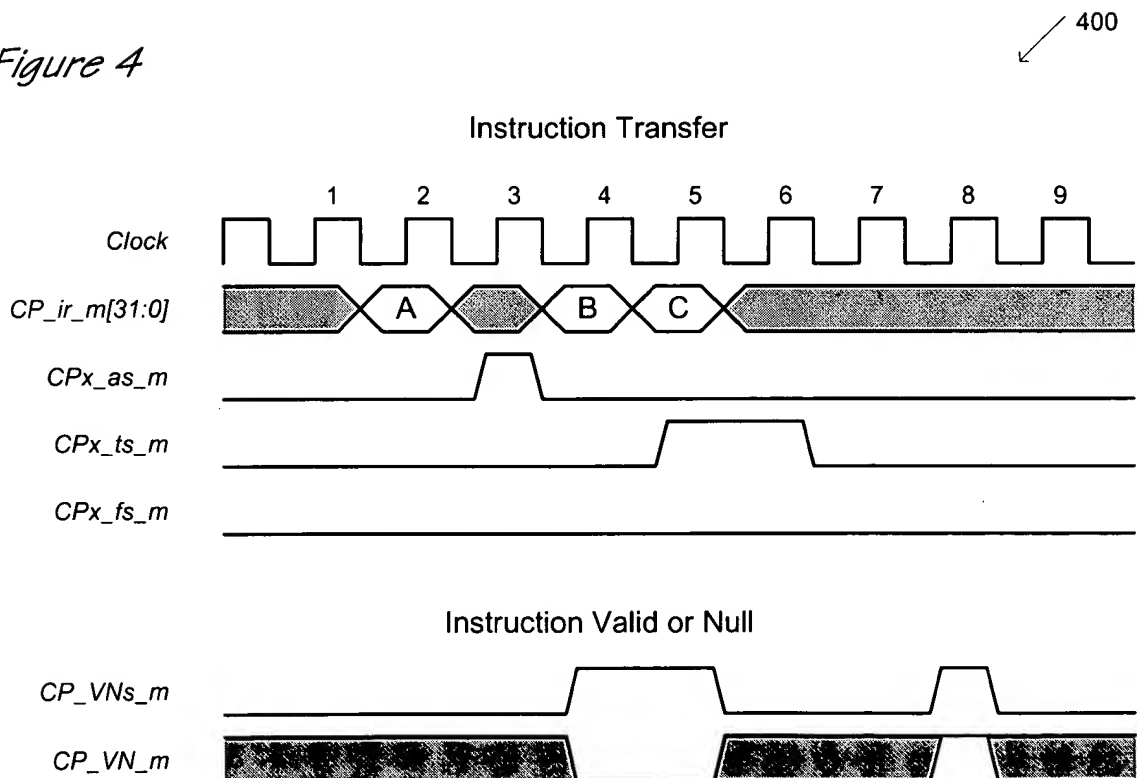
Instruction Transfer-Multiple Issue Groups

	1	2	3	4	5	6	7	8	9
Clock									
CP_ir_0[31:0]	A			D		E			
CP_ir_1[31:0]	B		C				F		
CP1_as_0									
CP1_as_1									
CP1_ts_0									
CP1_ts_1									
CP_order_0[2:0]		0			1		0		
CP_order_1[2:0]		1			0			0	

Figure 6

/ 600
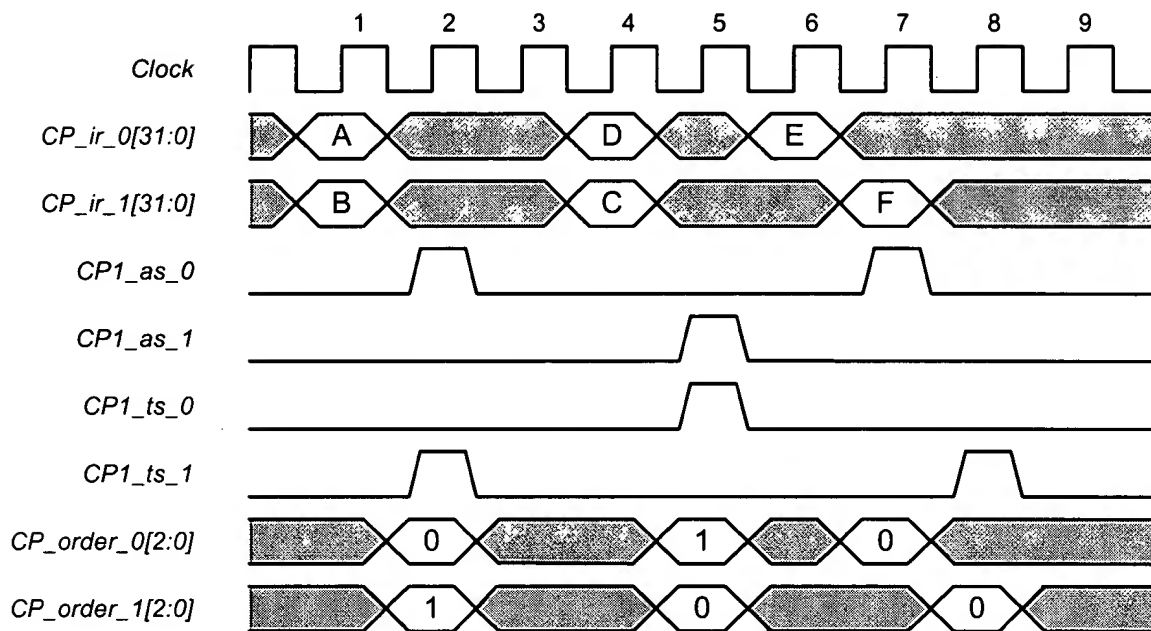
Instruction Transfer-COProcessor Busy

	1	2	3	4	5	6	7	8	9
Clock									
CP_ir_0[31:0]	A		B			C			
CPx_as_m									
CPx_ts_m									
CPx_fs_m									
CPx_abusy_m									
CPx_tbusy_m									
CPx_fbusy_m									

Figure 7

To/From COProcessor Data

700

Figure 8

800

To COProcessor Data Transfer

Figure 9

900

From COProcessor Data Transfer

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

Clock

CP_ir_m[31:0] — A B C D

CPx_fs_m

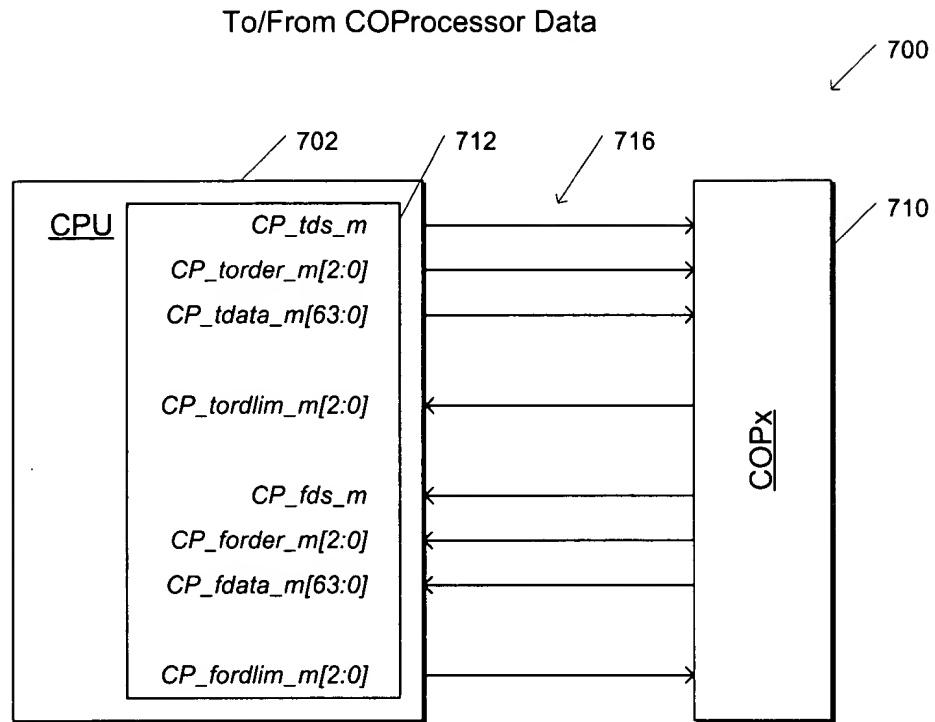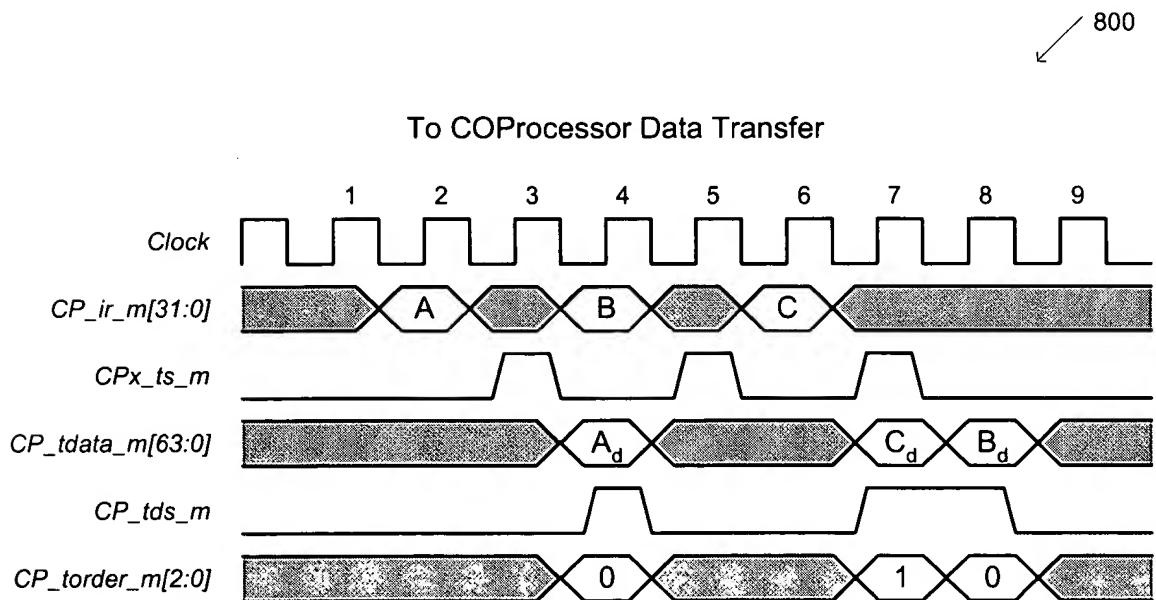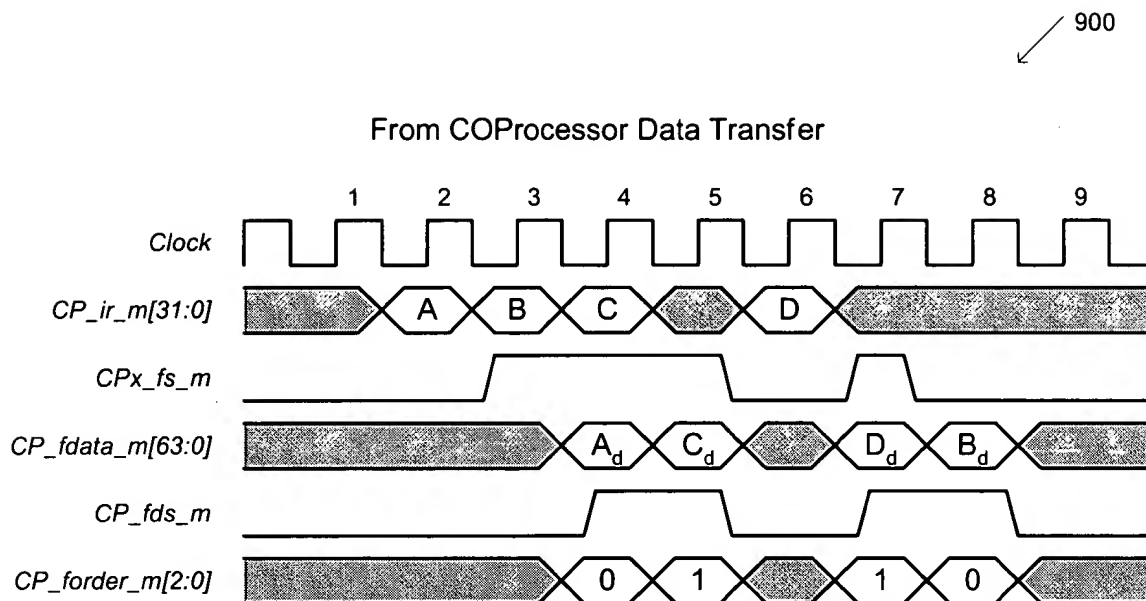CP_fdata_m[63:0] — A_d C_d D_d B_d

CP_fds_m

CP_forder_m[2:0] — 0 1 1 0
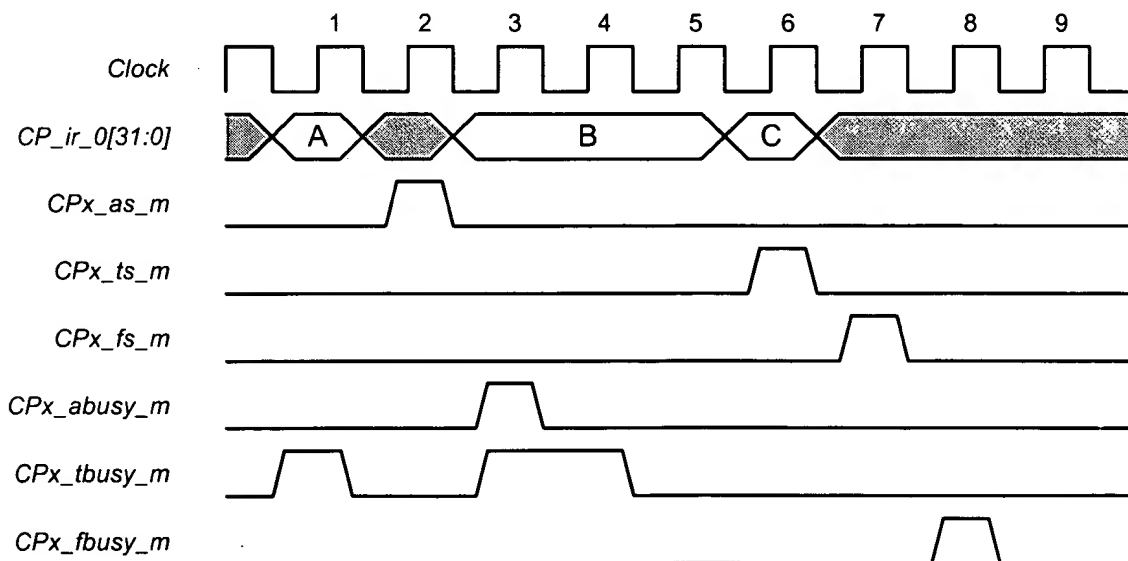
Figure 10

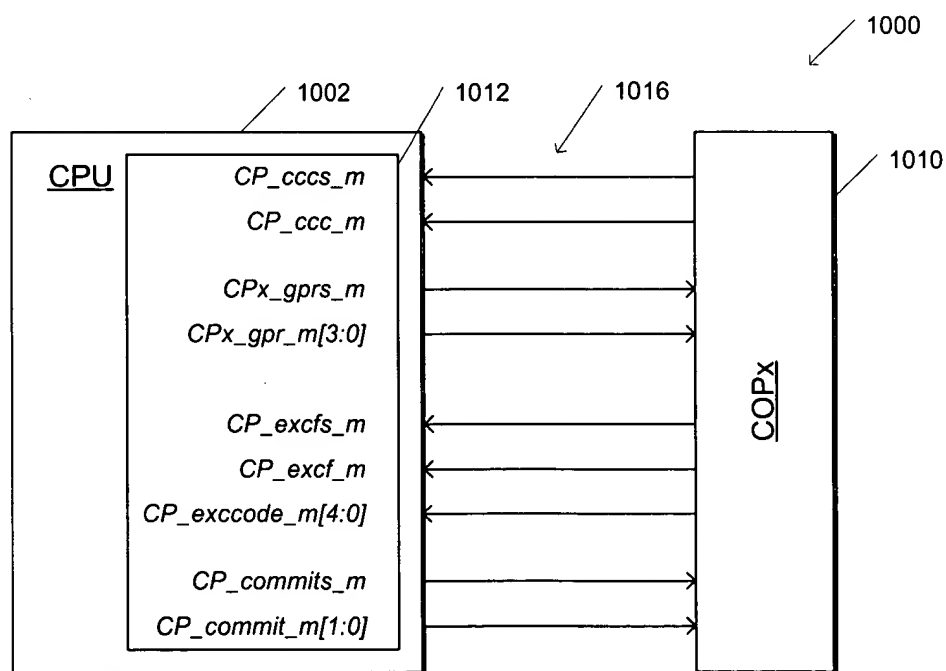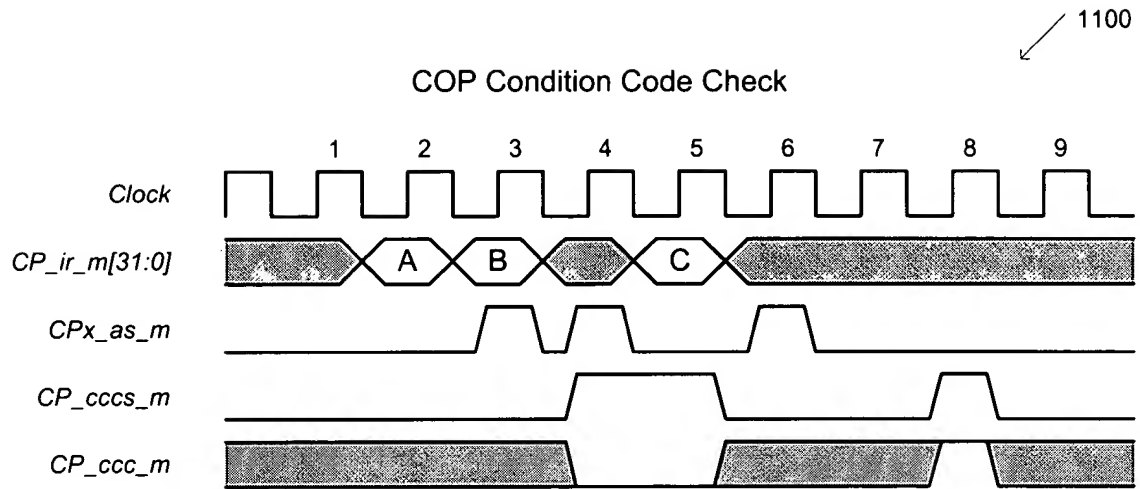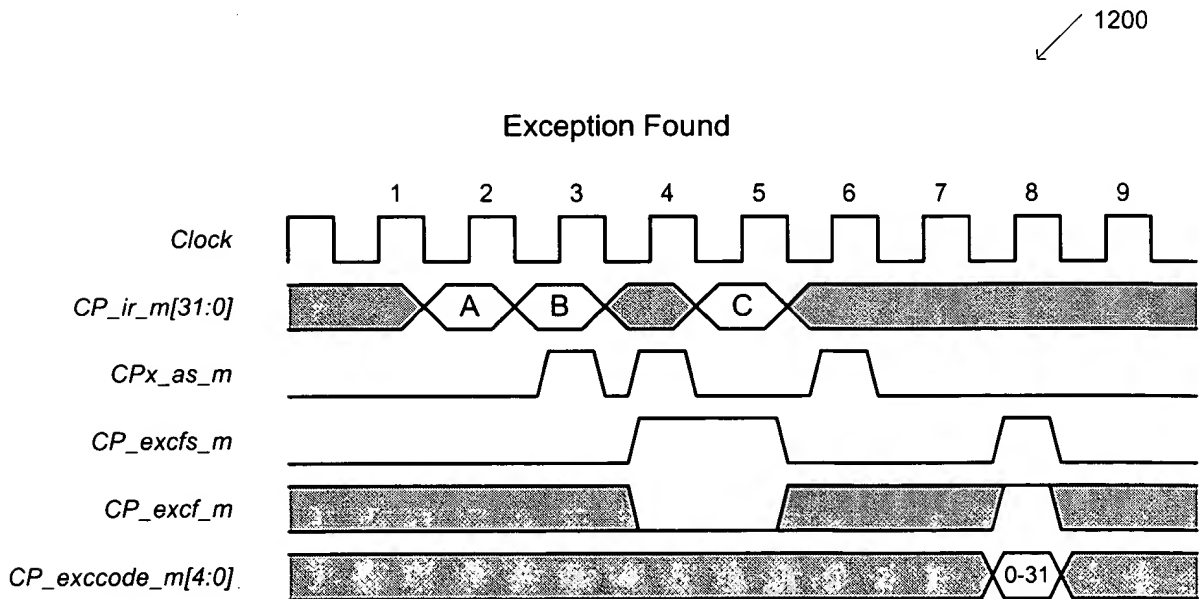**COProcessor Condition Code Check / GPR / exception Found / Instruction Commit**

1000

1002   1012   1016

CPU   1010

CP_cccs_m

CP_ccc_m

CPx_gprs_m

CPx_gpr_m[3:0]

CP_excfs_m

CP_excf_m

CP_exccode_m[4:0]

CP_commits_m

CP_commit_m[1:0]

COPx

Figure 11

/ 1100

COP Condition Code Check

	1	2	3	4	5	6	7	8	9
Clock									
CP_ir_m[31:0]		A	B		C				
CPx_as_m									
CP_cccs_m									
CP_ccc_m									

Figure 12

/ 1200

Exception Found

	1	2	3	4	5	6	7	8	9
Clock									
CP_ir_m[31:0]		A	B		C				
CPx_as_m									
CP_excfs_m									
CP_excf_m									
CP_exccode_m[4:0]								0-31	

Figure 13

Instruction Committing

1300